AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

What is claimed is:

1. (Original) A floating point accumulator, said accumulator comprising:

A first circuit network which is designed to convert floating point numbers expressed in base 2 format into floating point numbers expressed in a new base format represented by a whole number;

A second circuit network which is designed to compare the exponents of two of the converted numbers by comparing some number of most significant bits of the exponents of the two converted numbers, said bits representing exponent values of the two converted numbers;

A third circuit network which is designed to shift mantissas, add shifted mantissas of the two converted numbers using compressors, choose an accurate result mantissa, and partially normalize feedback mantissas;

A fourth circuit network designed to convert back to base 2 format both the mantissa and exponent of the final result.

2. (Original) The floating point accumulator of claim 1, wherein said floating point numbers are converted into numbers expressed in a new base by shifting the mantissas of each floating point number by a quantity equal to the K least significant bits of the exponents of the floating point numbers and by removing the K least significant bits from the exponents, where K equals the logarithm to the base 2 of the new base.

3. (Original) The floating point accumulator of claim 2, wherein said accumulator includes at least two registers, including an exponent register storing a first exponent value and a feedback exponent register that initially stores a second exponent value and that is updated periodically with a feedback exponent value.

4. (Original) The floating point accumulator of claim 3, wherein a comparator compares the exponent values each stored in one of the exponent registers and transmits a control signal indicating the larger of the two exponent values.

5. (Original) The floating point accumulator of claim 4, wherein a first multiplexer receives said control signal and said exponent values and transmits the larger of the exponent values.

6. (Original) The floating point accumulator of claim 5, wherein a plurality of adding devices receive said exponent values, calculate a plurality of augmented values each equal to the sum of one of the values and one and transmit the augmented values.

7. (Original) The floating point accumulator of claim 6, wherein a second multiplexer receives said augmented values and said control signal and transmits the larger of the augmented values.

8. (Original) The floating point accumulator of claim 7, wherein a third multiplexer receives the augmented value transmitted by the second multiplexer, the value

transmitted by the first multiplexer, and an control signal which selects either the value transmitted by the first multiplexer or augmented value transmitted by second multiplexer.

9. (Original) The floating point accumulator of claim 8, wherein a fourth multiplexer receives said exponent values, another of said exponent values reduced the whole number amount by a subtracting device, and an overflow control signal which causes the greater of the values received by the fourth multiplexer to be transmitted if a sum of the shifted mantissas of the floating point numbers exceeds the mantissa size supported by said accumulator, otherwise the fourth multiplexer transmits the smaller value it receives.

10. (Original) The floating point accumulator of claim 9, wherein a fifth multiplexer receive the value transmitted by the fourth multiplexer, the value transmitted by the third multiplexer, and a control signal, and selects the value transmitted by the fourth multiplexer if the feedback exponent value is greater than first exponent value by one or two and there are more than 31 leading zeros or ones in the feedback mantissa, otherwise the fifth multiplexer transmits the value received from the third multiplexer.

11. (Original) The floating point accumulator of claim 10, wherein a sixth multiplexer receives the value transmitted by the fifth multiplexer, the first exponent value, and a control signal that causes the first exponent value to be transmitted from the sixth multiplexer if all bits of a feedback mantissa are zero, otherwise the sixth multiplexer transmits the value transmitted by the fifth multiplexer.

12. (Original) The floating point accumulator of claim 11, wherein the values transmitted from the sixth multiplexer are transmitted to the feedback exponent register in a feedback loop and replace the value previously stored in the feedback exponent register during the last execution of the second circuit network.

13. (Original) The floating point accumulator of claim 12, wherein a first mantissa is received by and stored in a mantissa register and a second mantissa is received by and stored in a feedback mantissa register that are components of said third circuit network.

14. (Original) The floating point accumulator of claim 13, wherein the first mantissa is transmitted to a first shifter and is shifted right by a number of bits equal to the base of the numbering system in which the mantissas are added if the feedback exponent is greater than the first exponent.

15. (Original) The floating point accumulator of claim 14, wherein the second mantissa is transmitted to a second shifter and is shifted right by a number of bits equal to the base of the numbering system in which the mantissas are added if the first exponent is greater than the feedback exponent.

16. (Original) The floating point accumulator of claim 15, wherein said first mantissa is transmitted to a third shifter and said second mantissa is transmitted to a fourth shifter and said first mantissa is shifted right by the third shifter by a number of bits equal to the base of the numbering system in which the mantissas are added if the first exponent is

less than the feedback exponent by two, and said second mantissa is shifted left by a number of bits equal to the base of the numbering system in which the mantissas are added.

17. (Original) The floating point accumulator of claim 16, wherein said first and second mantissas are added by a first adding device in the mantissa loop forming a mantissa sum that is shifted right by a number of bits equal to the base of the numbering system in which the mantissas are added if the mantissa sum contains more significant bits than are supported by the accumulator.

18. (Original) The floating point accumulator of claim 17, wherein the mantissa sum is transmitted by a selecting multiplexer if the first and second exponents differ by one or if the exponents are equal, and otherwise the mantissa associated with the larger exponent is transmitted by the selecting multiplexer.

19. (Original) The floating point accumulator of claim 18, wherein a leading zero anticipator generates a signal that indicates whether the number of leading zeroes or ones contained in the second mantissa is equal or greater than the base of the numbering system in which accumulation is performed and is a portion of the control signal used to control said fifth multiplexer in the second circuit network.

20. (Original) The floating point accumulator of claim 19, wherein a second adder in said third circuit adds the shifted values generated by the third and fourth shifters and transmits the calculated sum to a sixth shifter that shifts the sum to the right by the base

of the number system in which mantissas are added if a mantissa overflow condition occurs when the mantissa sum is calculated.

21. (Original) The floating point accumulator of claim 20, wherein a third multiplexer in the mantissa loop receives the bit stream transmitted by the sixth shifter and the bit stream transmitted by second multiplexer in the mantissa loop and transmits the bit stream received from the sixth shifter if the feedback exponent value is greater than first exponent value by one or two and the number of leading zeroes or ones in the feedback manitssa is equal or greater than the base of the numbering system in which accumulation is performed.

22. (Original) The floating point accumulator of claim 21, wherein the base of the number system in which the mantissas and exponents of the floating point numbers are added is at least 32 for single precision format and at least 64 for double precision format.

23. (Original) The floating point accumulator of claim 22, further comprises a post normalization circuit wherein components of a mantissa result are added, shifted to remove leading zeroes, and shifted to convert the mantissas back into a number expressed in base 2 format, and the exponent result is increased or decreased by an amount that converts it back to base 2 format.

24. (Currently Amended) A method of adding floating point numbers, said method comprising:

Converting, using a first circuit network, the floating point numbers expressed in base 2 format into floating point numbers expressed in a second base format represented by a whole number;

Comparing, using a second circuit network, the exponents of two of the floating point numbers by comparing some number of the most significant bits of the exponents of the two floating point numbers, said bits representing exponent values of the two converted floating point numbers and choosing a correct result exponent;

Shifting and adding mantissas of two of the floating point numbers using one or more compressors and choosing a correct result mantissa using a third circuit network;

Repeating said comparing, shifting and adding multiple times using two of the floating point numbers, wherein one of the floating point numbers consists of a result exponent and result mantissa previously determined;

Converting, using a fourth circuit network, the result mantissa and exponent back to base 2 format.

25. (Original) The method of claim 24 further comprises storing an exponent value of a first floating point number in an exponent register and an exponent values of a second floating point number in an exponent feedback register that is updated periodically with a feedback exponent value produced by said comparison of exponent.

26. (Original) The method of claim 25, wherein a first mantissa is received by and stored in a mantissa register and a second mantissa is received by and stored in a feedback mantissa register that is updated periodically with a feedback mantissa value produced by said shifting and adding of mantissas.

27. (Original) The method claim 26 further comprises a zero detector that detects whether all bits of the feedback mantissa stored in the feedback mantissa register are zero.

28. (Original) The method of claim 27 further comprises a post normalization circuit wherein components of a mantissa result are added, shifted to remove leading zeroes, and shifted to convert the mantissas back into numbers expressed in base 2 format, and the exponent result is increased or decreased by an amount that converts it back to base 2 format.

29. (Withdrawn)

30. (Withdrawn)